Forming Virtual Traces for WCET Analysis and Reduction

Jack Whitham and Neil Audsley

August 27th 2008
Propose CPU modifications for:

1. accurate worst case execution time (WCET) analysis.
Goal of this work

Propose CPU modifications for:

1. **accurate worst case execution time (WCET) analysis.**
   
   ![Diagram](image)

2. **improved guaranteed throughput** (versus a simple CPU).
   
   ![Diagram](image)

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Requirements

The CPU modifications must:

- accommodate speculative and superscalar out-of-order operation so that throughput can be increased versus a simple CPU, and

\[ T = 0 \quad T = \text{WCET}_1 \quad T = \text{WCET}_2 \]

True WCET2 True WCET1
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- restrict this operation so that:
  - timings can be determined safely by measurement, and
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- accommodate speculative and superscalar out-of-order operation so that throughput can be increased versus a simple CPU, and
- restrict this operation so that:
  - timings can be determined safely by measurement, and
  - the WCET analysis model won’t include any *pessimistic* assumptions.
A trace

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In this work, every trace has two forms:

1. executable code that implements some machine code within a program; often more than one basic block.
2. a timing model that gives precise information about path timings through that code.
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How do traces meet the requirements?
Previous work

In previous work, we considered the use of a trace scratchpad to implement traces and meet the requirements, used as follows:

1. Take a program in machine code form;

- Apply WCET analysis to find the WCEP;
- Convert subsequences of the WCEP into traces implemented by microcode. These are explicitly parallel and optimise execution for one path.

exit returns to machine code

trace entrance

trace exit trace exit

trace implemented using microcode

(a) (b)

microcode

BB4
BB5BB2
BB3BB1 BB6 BB1,3,6
BB4
BB5BB2

Jack Whitham and Neil Audsley () Forming Virtual Traces for WCET Analysis August 27th 2008 5 / 23
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4. Allocate space in a trace scratchpad for microcode. The microcode is used in place of the original machine code.

A virtual trace is a compact encoding, specifying the execution path that should be assumed by the CPU.
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Virtual traces are theoretically equivalent to traces, but some practical problems are solved:
- the need for a custom CPU with a writable microcode store,
- the need for a CPU-specific compiler to generate microcode,
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- the need for a CPU-specific compiler to generate microcode,
- the poor code density of microcode.

Result: No microcode. The virtual trace controls a conventional but constrained dynamic CPU scheduler.
Regard the CPU dynamic scheduler as a decoder:

\[ \text{machine code} + \text{virtual trace} \rightarrow \text{microcode} \]
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2. Handle all events that could change execution times.
Benefits of virtual traces

Some are the same as for traces:

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But there’s more:

- Any CPU could be modified with the correct restrictions. Predictable mode could be optional.
- The CPU is its own timing model.
Problem (for this paper)

How do we turn a program (as a graph of basic blocks) into a graph of virtual traces traces?
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- **Previously**: due to limited trace scratchpad space, only *some* parts of the program could be translated. A specialized search algorithm was used to find the most suitable WCEP subsequences.
- **Now**: space limit is less restrictive, so the whole program should be translated.
- This problem is similar to selecting static branch predictions to minimize WCET.

Proposed solution

Combine two algorithms:
- Bodin-Puaut static branch prediction scheme.
- Trace formation algorithm from previous work.
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Combine two algorithms:

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  1. Assume all branches are *unknown*;
  2. Use WCET analysis to find the WCEP through the program;
  3. Assign *unknown* branches to follow the WCEP.
     If any *unknown* branches were found, go to 2.

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- Trace formation algorithm from previous work.
  - Form traces by following branch predictions.
Example
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$L$, the maximum virtual trace length.  
(The number of branch predictions stored in each virtual trace.)
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- Defined by the size of the memory for virtual traces.
- $L = 1 \Rightarrow$ Trivial traces: like assuming all branches are unknown.
- $L > 1 \Rightarrow$ Non-trivial traces: speculation is used to reduce the cost of the predicted execution path.
Experiment 1

What is the relationship between trace length and WCET?
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- Compare $L = 1$ against $L \in [4, 8, 12, 16]$ for various benchmark programs.
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- Compare $L = 1$ against $L \in [4, 8, 12, 16]$ for various benchmark programs.
- Using experimental platform from:

Normalized against results for $L = 1$. 
Experiment 2

The Bodin-Puat algorithm never changes any branch predictions once made... is an opportunity for improvement being lost?
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1. Try flipping each branch prediction in each program, i.e. not taken $\leftrightarrow$ taken, and evaluate the new WCET in each case.
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1. Try flipping each branch prediction in each program, i.e. not taken ↔ taken, and evaluate the new WCET in each case.

2. If an improvement is found, repeat step 1.
### Results 2

<table>
<thead>
<tr>
<th>Program</th>
<th>$L = 4$</th>
<th></th>
<th>$L = 16$</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>i</td>
<td>NW</td>
<td>%ch</td>
<td>i</td>
</tr>
<tr>
<td>cnt</td>
<td>1</td>
<td>0.679</td>
<td>0.1%</td>
<td>1</td>
</tr>
<tr>
<td>compress</td>
<td>3</td>
<td>0.604</td>
<td>0.2%</td>
<td>2</td>
</tr>
<tr>
<td>edn</td>
<td>2</td>
<td>0.629</td>
<td>0.5%</td>
<td></td>
</tr>
<tr>
<td>expint</td>
<td>1</td>
<td>0.668</td>
<td>0.0%</td>
<td>1</td>
</tr>
<tr>
<td>fibcall</td>
<td>1</td>
<td>0.616</td>
<td>16.8%</td>
<td>1</td>
</tr>
<tr>
<td>janne_complex</td>
<td>2</td>
<td>0.675</td>
<td>6.7%</td>
<td>2</td>
</tr>
<tr>
<td>matmult</td>
<td>2</td>
<td>0.677</td>
<td>0.1%</td>
<td>2</td>
</tr>
<tr>
<td>ndes</td>
<td>4</td>
<td>0.669</td>
<td>0.1%</td>
<td>5</td>
</tr>
<tr>
<td>ns</td>
<td>3</td>
<td>0.305</td>
<td>7.9%</td>
<td>2</td>
</tr>
</tbody>
</table>
Related Work

- Scratchpads
  \textit{Puang, Suhendra, Wehmeyer}

- Single-path paradigm
  \textit{Puschner}

- Hybrid timing analysis
  \textit{Mohan, Mueller}

- Dataflow-like computing models
  \textit{Lee et al.}
Implementation

[Diagram showing the flow of data and instruction processing through the fetch unit, dynamic scheduler, and execution units.]

- **Fetch unit**: Instruction cache and memory i/face
- **Dynamic Scheduler**: Load/store unit, data cache and memory i/face
- **Execution units**: VTR, Memory for encoded virtual traces
- **Instruction scratchpad and memory i/face**: Instruction cache and memory i/face
- **Data cache and memory i/face**: Conventional CPU component with minor changes
- **VTC**: New component, replacement for conventional cache

The diagram illustrates the flow of operations from fetch unit to execution units, highlighting the integration of virtual traces (VTR) for efficient memory access and execution.
Virtual traces improve on scratchpad traces by allowing an entire program to be executed in trace form with a low storage cost for the trace data.
Conclusion

- Virtual traces improve on scratchpad traces by allowing an entire program to be executed in trace form with a low storage cost for the trace data.
- Consequently, greater WCET reductions are possible.
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The Bodin-Puaut algorithm is not optimal but only minor improvements are possible.
All questions and comments are welcome!

Further information:
http://www.jwhitham.org.uk/pubs/